A Dual Edge Triggered Flip Flop for Low Power Applications

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Abstract- Among many techniques of power reduction the technique of power gating is used considering the different modes of operation of flip flop. In the proposed flip sleep mode and idle mode are used maintaining their state of data retention having pulse triggering on both edges rising and falling, of the clock. The circuit has used low threshold voltages so as to operate at low V_{dd} .The simulation of the circuit is done using tanner tool in 45nm technology. The comparison of the proposed circuit, when done with the DETFF1 and DETFF2 operated at 0.5V, the proposed latch has 72% power saving.

Keywords- *Power gating, State retention, Threshold region*

I. INTRODUCTION

In present days, power consumption has attracted much interest in VLSI circuit design. There are many tasks to optimize the power consumption. Designing low power logic is one of the most important techniques in this case. Practically, latch and Flip-Flop (FF) is extremely used in VLSI design of D-Flip-Flops (DFF) such as load capacitance of the clock, delay from the edge of clock to output of DFF, and the area. Also, tradeoff between speed and power consumption should be considered in design of digital circuits. Clock signal is needed for the synchronization of large number of digital components, the clock load increases substantially. The clock network alone dissipates 30-70% of the total system power dissipation hence reduction in power dissipation due to clock load has been a major area of emphasis for digital system designers. One of the most effective methods to reduce both dynamic power consumption and leakage power consumption is to reduce the supply voltage.

II. DUAL EDGE RIGGERED FLIP FLOP

A. Introduction

Flip flop, to a large extent, determine the speed of synchronous system and in a dual edge triggered flip flop same data throughput can be achieved with half of the clock frequency as compared to single edge triggered flip flop.

B. Dual Edge Triggered Flip Flop Design 1

Following figure shows the Dual edge triggered for low power applications where D is the input of the flip flop having Q as output. The transistors P1, N1, N2, N3 consists an inverter having D input and X output. This flip flop will operate in active region only when D and Q will differ from each other.

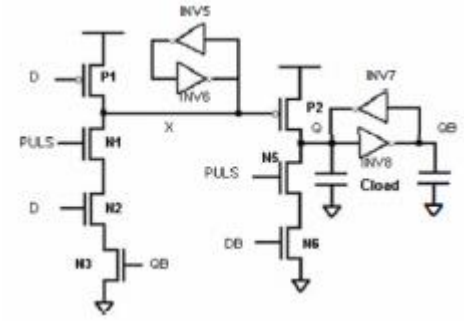

Fig1. Dual edge triggered flip flop design 1

C. Dual Edge Triggered Flip Flop Design 2

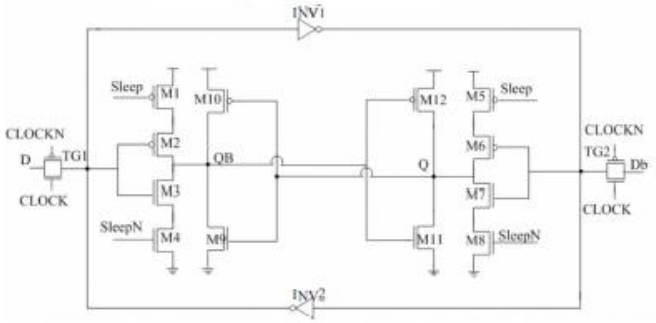

Fig 2: Dual edge triggered Flip Flop design 2

1. Features

The above figure shows a DEFTT triggered by external pulse where CLK is the regular clock signal. but CLKB is the delayed version of regular clock signal. The pulse is generated by two transmission gates TG1 and TG2 in which TG1 is enabled by CLKB and TG2 is enabled by inverted CLKB signal

2. Principle

The above circuitry has different operational modes. During active mode of operation when the Sleep signal is low then in the transparent mode CLK is provided 1 then both the transmission gates allow the data to be latched and the transistors M1-M4 and M5-M8 are responsible for the biasing of output node Q and QB to their correct state. For storage of the data inverters INV1 and INV2 and transistors M9-M10 and M11-M12 are present there during static mode. During sleep mode or retention mode i.e. when the sleep signal is high some transistors are switched off to save

the power consumption retaining the logic state using those transistors which are not affected by sleep signal. So M1, M4, M5 and M8 are switched off and M6, M7, M2 and M3 are cut off from the power supply so as to reduce the power dissipation

III. PROPOSED FLIP FLOP DESIGN

As explained earlier that the previous DETFF design 1 power reduction was done by switching off some of the transistors. Mainly power consumption increased by increasing the number of transistors in a circuit, so to reduce the power consumption the proposed design has lesser number of transistors

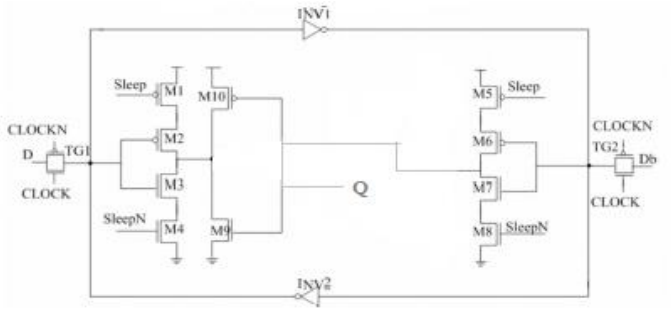

Fig.3: Proposed design

In the earlier circuit the power was consumed by the transistors M9, M10, M11 and M12 during the activation of sleep signal, so in the proposed design of flip flop. The transistors M9 and M10 are removed since when the sleep signal will be high, the power consumption will be due to 2 transistors that are M11 and M12 and not from all the 4 transistors M9-M12 when operated at 0.5V and when the sleep signal will be low again the circuit state and normal functioning of the flip flop is retained

IV. SIMULATION AND ANALYSIS

A. *Performance of Dual edge triggered designs*

The performance of proposed circuit was evaluated tanner tool using 45nm technology with 0.5v supply voltage. The comparison of the proposed flip flop and the previous designs of flip flop have been held by taking voltage 0.5V.The previous design 2 is having output waveform as shown in fig. 4

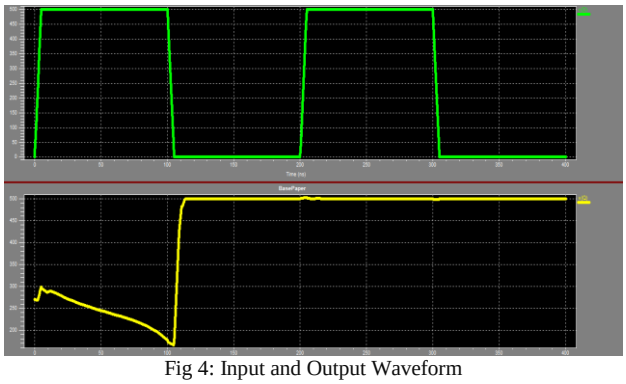

Fig 4: Input and Output Waveform

The operation of proposed circuit is shown below with the help of diagram. The output of D flip Flop follows the input when there is less power dissipation.The power consumption for the proposed circuit comes out to be 72% less than the previous design of DETFF when operated at 0.5V.

B. *Waveform of proposed design*

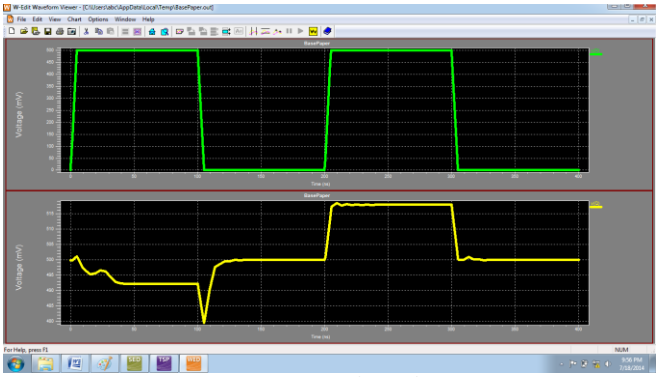

Fig. 5: Input and Output Waveform of proposed design

C. *Tables.*

Power dissipation of DETFF-1 and 2, Table III shows Power dissipation of proposed design and Table IV of parameters

TABLE I. POWER DISSIPATION (WATTS)

Voltage(V)	Power dissipation(Watts)
0.3	9.2e-03
0.5	1.38e-02
0.7	7.9e-03
0.9	1.9e-02

TABLE II. POWER DISSIPATION (WATTS)

Voltage(V)	Power dissipation(Watts)
0.3	7.98e-08
0.5	3.64e-05
0.7	2.16e-03
0.9	1.56e-02

TABLE III. POWER DISSIPATION (WATTS) OF PROPOSED DESIGN

Voltage(V)	Power dissipation(Watts)
0.3	1.2e-04
0.5	6.2e-05
0.7	2.8e-03
0.9	1.50e-02

TABLE IV. PARAMETERS

Factors	DETFF design 1	DETFF design 2	Proposed design
Power dissipation	1.38e--002	6.28e--005	3.64e--005
Time delay	6.17e-+008	2.29e-+008	1.23e-+009
Power delay product	8.51e-+006	14.38e-+003	4.47e-+004

V. CONCLUSION

As technology scales down operation at low power supply with less power consumption has become the ultimate priority. A low-power near threshold state retentive pulsed latch was proposed and developed at 45nm technology node. The proposed circuit was operative at very low voltages of up to 0.5 V and is also state retentive. The PDP savings was compared with other state retentive latches and the proposed circuit came out as the best. The operation of the circuit for both the active mode and the sleep mode were tested for correctness. The design-2 circuit has PDP savings at 0.9V as 87.8%. When the proposed circuit operates at 0.5 V, it has PDP savings as 78.26 %. In the modified circuit the voltage when going to increase correspondingly then the power consumption is also increased up to a certain level. But as compared to dual edge triggered design 1 and 2 the power consumption is highly reduced at each voltage level when simulated at 45nm technology. The proposed circuit and developed at 45nm and 32nm technology and was operated at low voltages. The proposed flip flop has 72% less power consumption at voltage 0.5V.

VI. REFERENCES

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